

1004787-030400

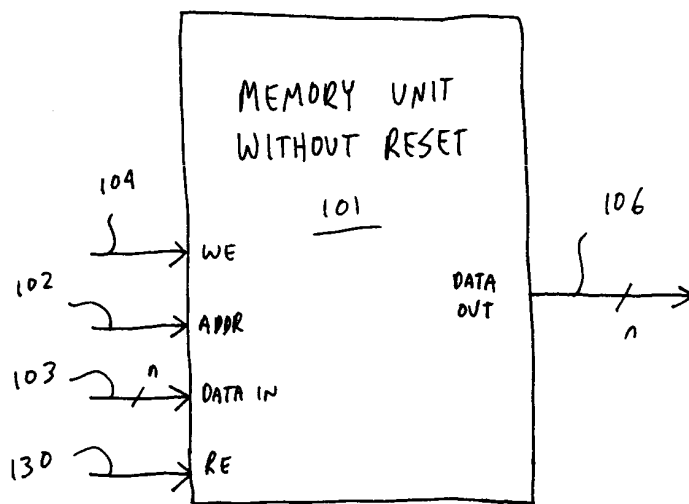


FIGURE 1

# REPORT

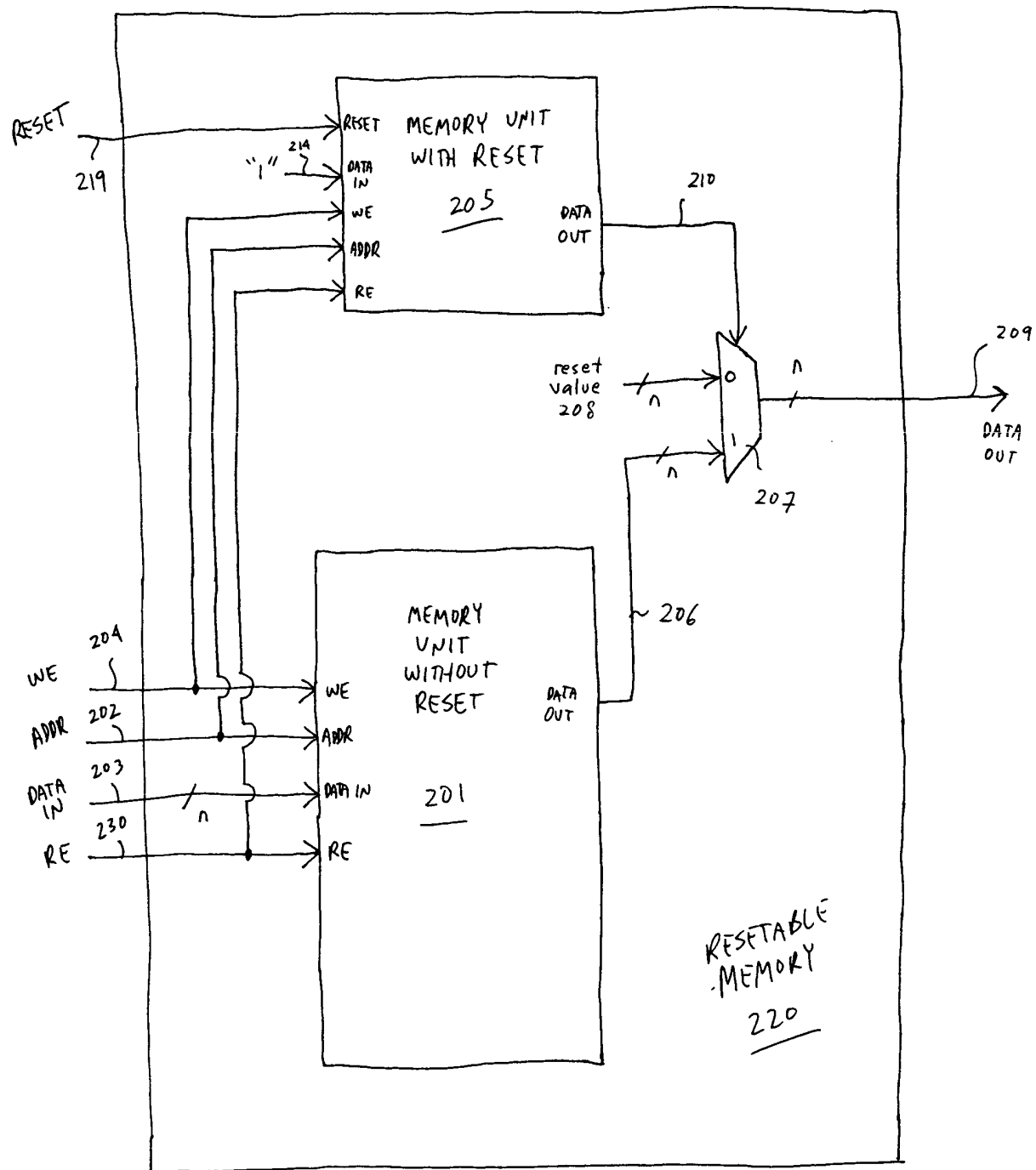


FIGURE 2A

2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100

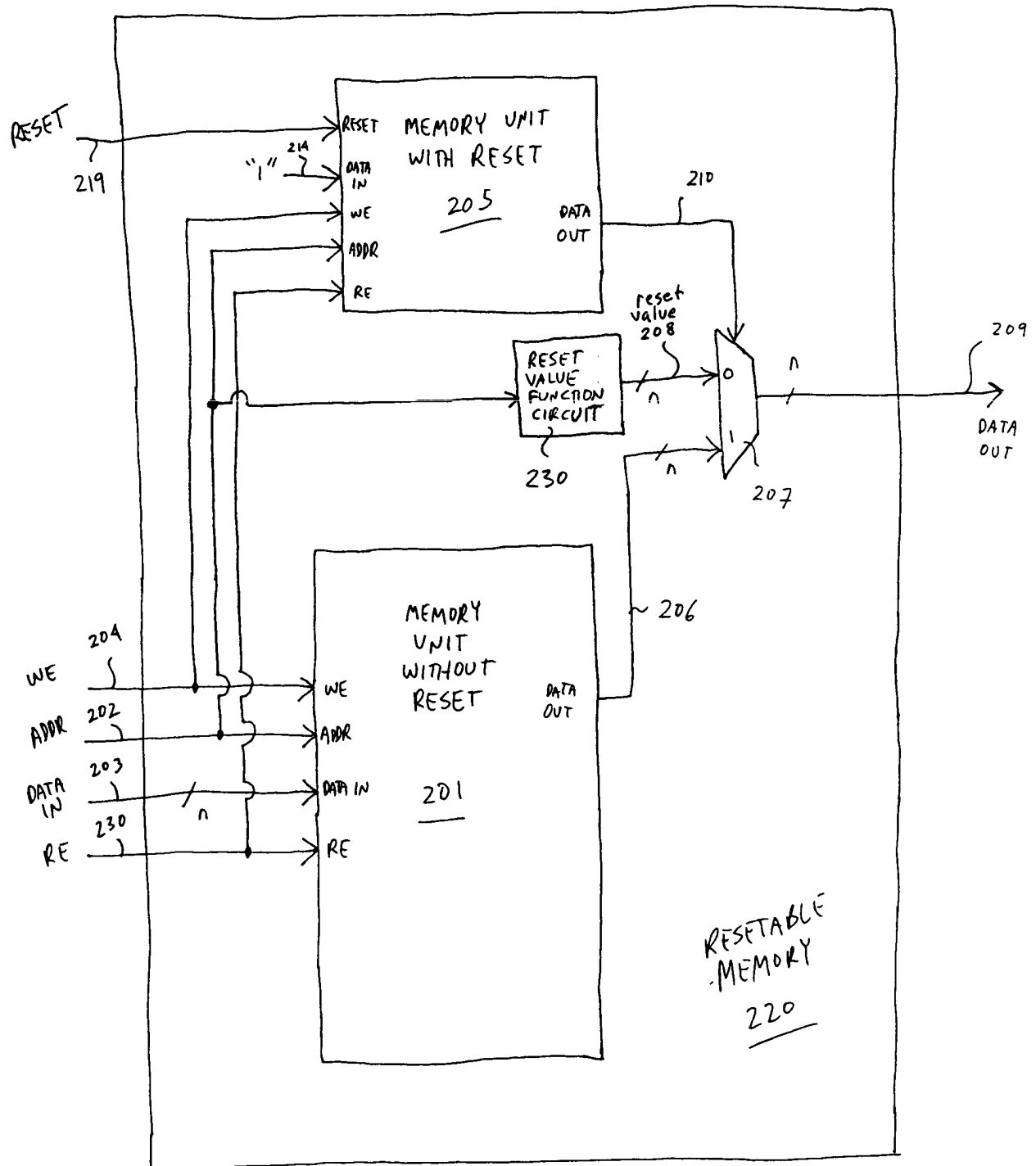


FIGURE 2B

**module** synReset(data\_in, addr, reset, we, clk, data\_out);

**parameter** data\_width = 1024;

**parameter** addr\_width = 10;

**parameter** RAMsize = 8;

**parameter** reset\_value = 8'D0;

**input** [data\_width-1:0] data\_in;

**input** [addr\_width-1:0] addr;

**input** reset, we, clk;

**output** [data\_width-1:0] data\_out;

**integer** i;

**reg** [data\_width-1:0] mem [RAMsize-1:0];

**wire** [data\_width-1:0] data\_out;

//synthesis loop\_limit 2000

**always** @(posedge clk)

**begin**

**if**(reset == 1'b1)

**begin**

**for** (i=0; i < RAMsize ; i=i+1)

**begin**

                    mem[i] = reset\_value;

**end**

**end else if**(we == 1'b1)

**begin**

            mem[addr] = data\_in;

**end**

**end**

**assign** data\_out = mem[addr];

**endmodule**

FIGURE 2C

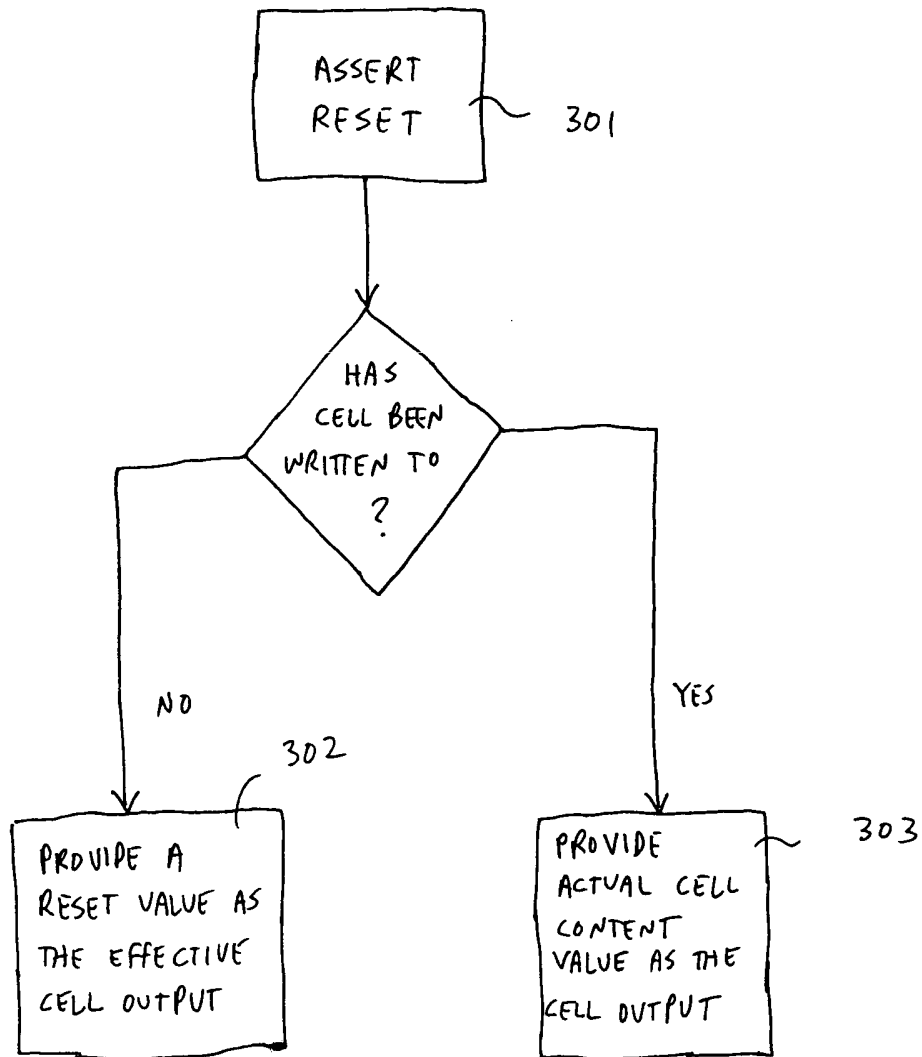


FIGURE 3

1004787-030403

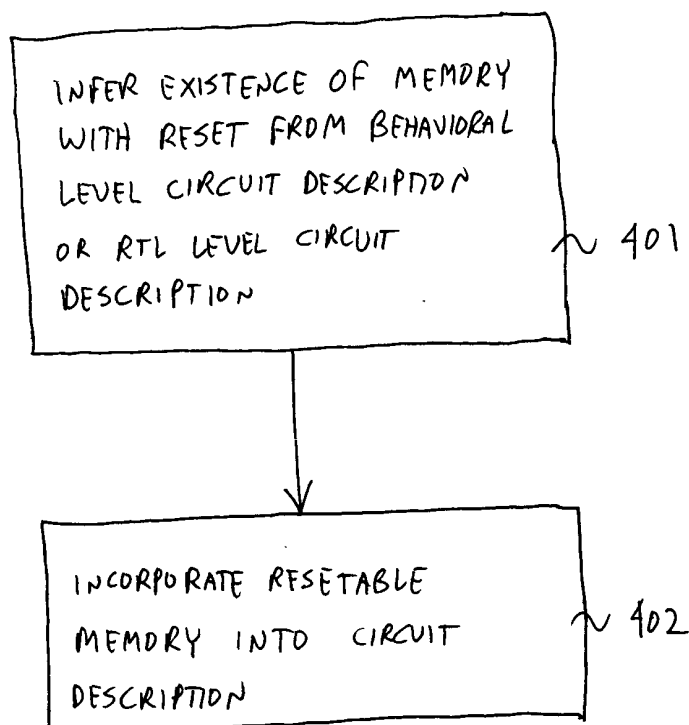


FIGURE 4

10091787-030402

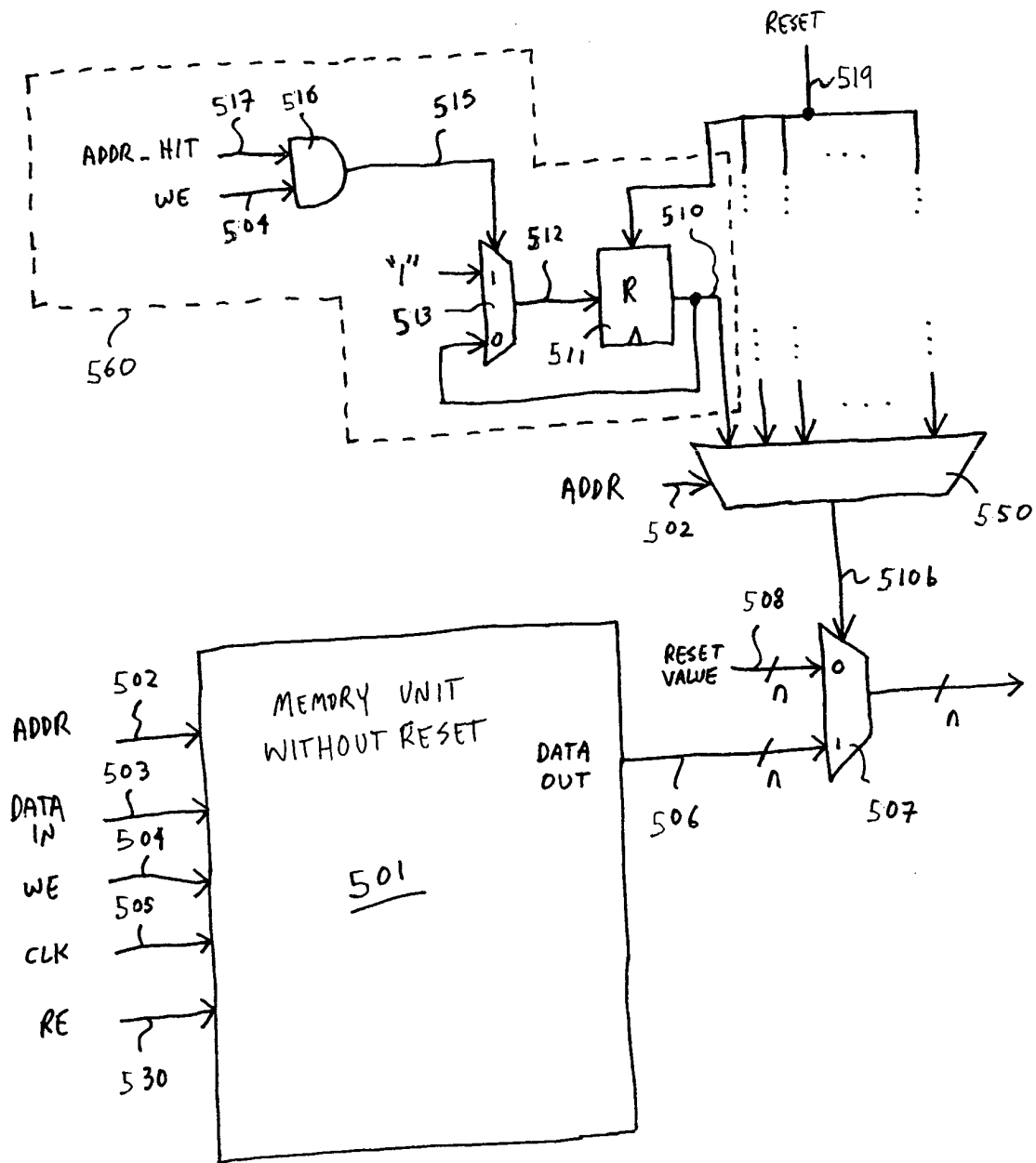


FIGURE 5.

10094787-030403

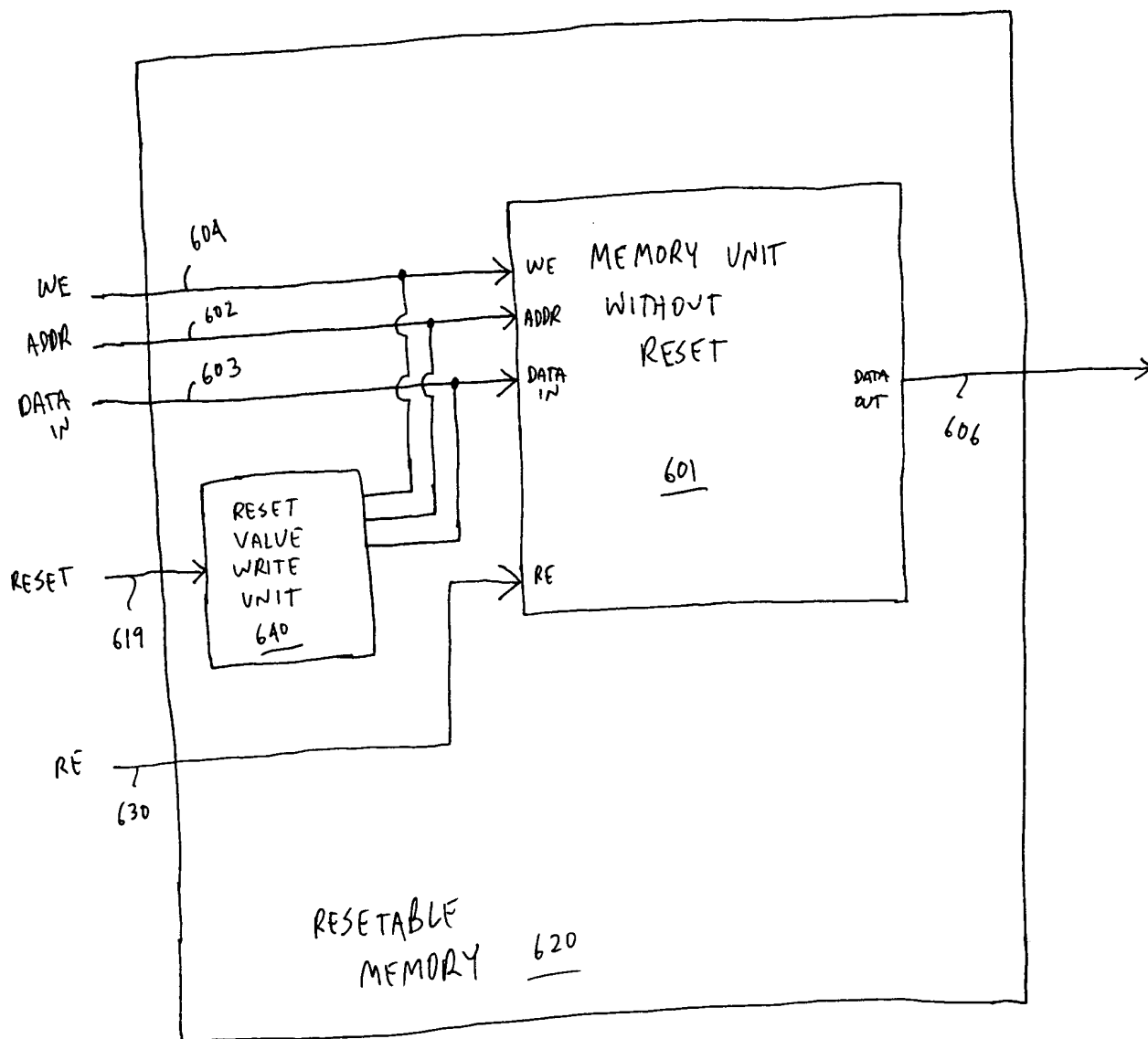


FIGURE 6



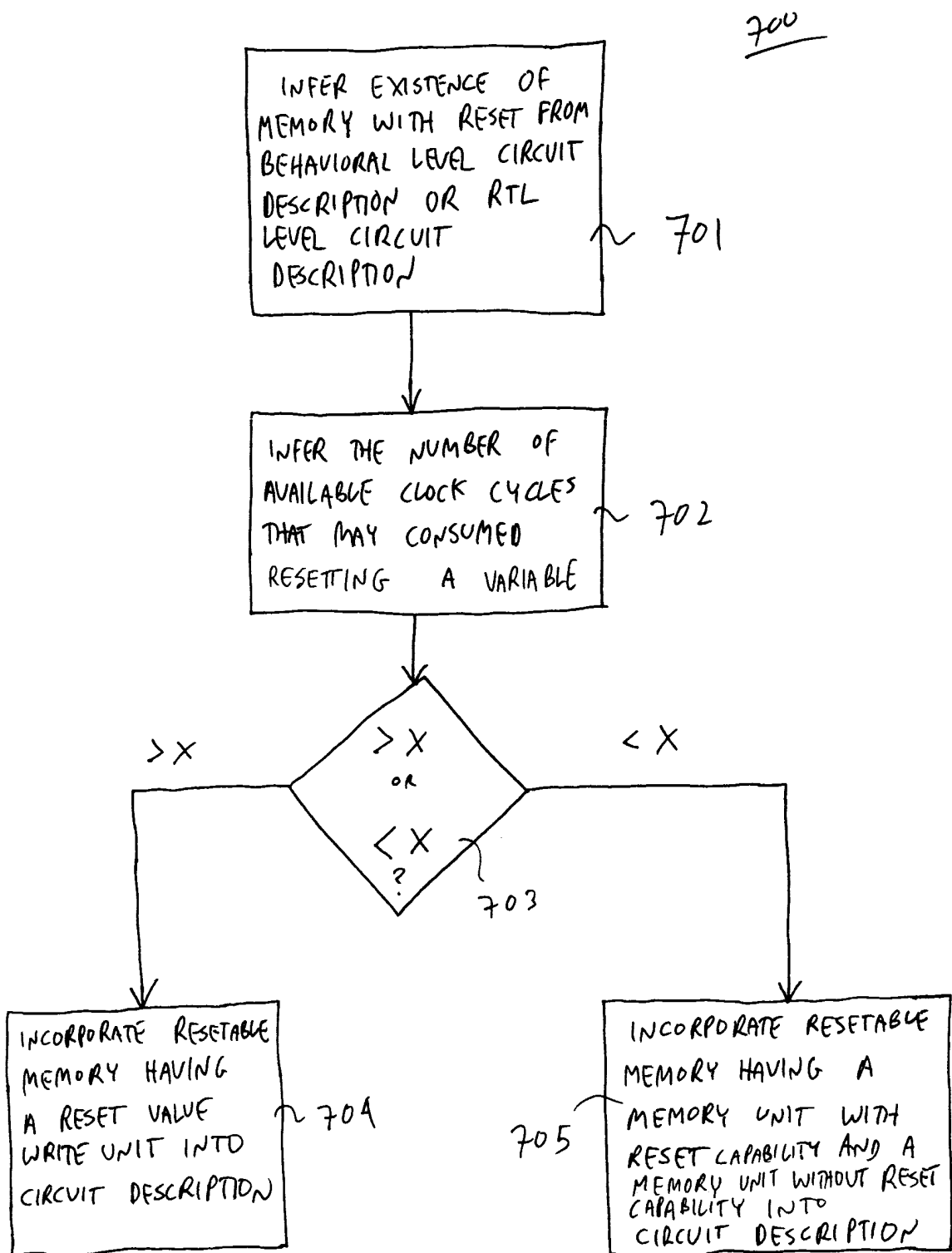


FIGURE 7

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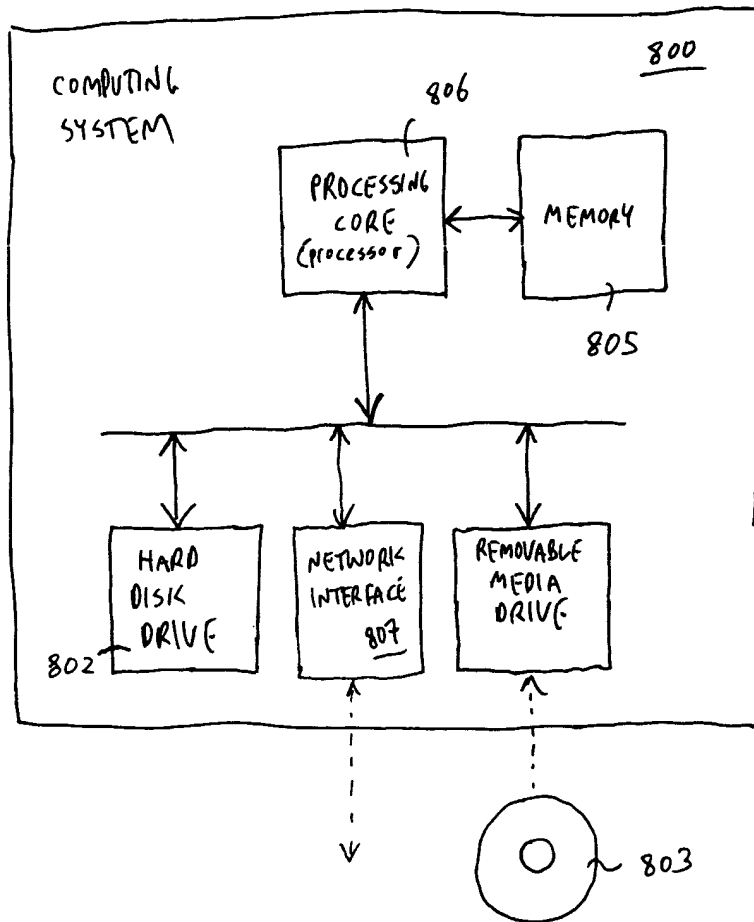


FIGURE 8